EMC Simulation Techniques for Printed Circuit Boards

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Electronic devices radiate electromagnetic signals when operating. Because electronic equipment is sensitive to electromagnetic fields, their normal operation can be disrupted by emissions from other devices. For reasons of functionality and safety, international standards have been established to ensure compliance of equipment under a variety of situations. In 1980 the U.S. Federal Communication Commission imposed regulations on commercial digital products and in 1992 the European Union imposed the CE mark requirement.

Amongst others, two very useful books on the subject are [1] and [2].

To be prudent, it is best to design the PCB layout with electromagnetic compatibility (EMC) in mind rather than to be faced with excessive emissions at the prototype stage or – worse still – just prior to production. Unfortunately, too many of the problems are uncovered at the testing stage. Shielding and absorbing materials are then often used to reduce the emissions.

A preferred approach is to identify the problems at the board level and to rectify them there. Even then, if particular offending frequencies are identified, engineers are still faced with the nightmare of locating which net segments are the cause of these particular emissions

The use of computer simulation prior to prototyping is one methodology that can be used to help reduce unwanted emissions and the number of laboratory tests required. The estimated fully burdened cost associated with producing a new board to test is roughly $10,000 per prototype. Time to market costs become even more significant than the tangible board turn costs as companies risk losing over 50 percent of overall potential profitability. Eliminating problems early in the design process will result in a significant saving in design irritations and accelerated time-to-market.

Once excessive emissions are detected at several frequencies, the goal is to quench these emissions. Crude and expensive techniques involve the design of sealed enclosures, chokes and ferrites to restrain the launching of common-modes along cables and a variety of other methods that are too little and too late. Alternatively, and more proactively, system developers recognise that the problem should be addressed at the board level. This application note discusses simulation techniques for the identification of the nets that are the cause of excessive emissions and signal integrity problems. Simple techniques are then available for the suppression of these emissions, e.g. the attachment of resistors to drivers and receivers.

Solution of the Electromagnetic Fields

Because of the high clock speeds on printed circuit boards, nets have to be treated as sets of transmission lines. This approach is needed when the signal delay times along the net begin to approach that of the signal rise times. What we observe is ringing due to multiple reflections from drivers and receivers, for example. To model the transmission lines, we need to obtain what are commonly called the parasitics associated with the tracks. In particular, we have to obtain mutual and self inductances, mutual capacitances between nets and to grounds, etc.

These electrical parameters are derived from the solution of the electromagnetic fields that surround tracks in proximity to one another and the adjacent power and ground planes. If the distances between adjacent wires and planes are small with respect to the fundamental and significant harmonic

wavelengths encountered, we can assume that the fields in the cross-section may be considered to be quasi-static, i.e. they obey the two-dimensional form of the Laplace equation. The basic assumption (a very good one) is that the magnitude of the electric and magnetic field components in the direction of the wires is negligible. What this is saying is that we don't have to consider waveguide modes. For the dimensions of present boards, this means that this assumption is valid for up to several gigahertz. As speeds increase, board track and spacing dimensions will surely decrease and so it is likely that these assumptions will always be valid. If not, the analysis will become more complex – but not impossible.

One approach is to define the field problem as the solution of the Laplace equation, whose simplest form is

$$\nabla^2\varphi(\mathbf{r}) = 0 \qquad (1)$$

where $\varphi(\mathbf{r})$ is the electric potential in volts (V) in the dielectric and air space $\mathbf{r}$ surrounding the tracks. To complete the definition of the problem, boundary condition (e.g. $\varphi(\mathbf{r})$) need to be stated.

The potential distribution is frequently solved by using the Finite Element Method (FEM) [3]. This requires that elements be constructed outward – in theory to infinity. However, in practice the region may be truncated at some finite distance by bounding the space with an impedance surface.

As an alternative, we may solve the integral equation

$$\int_s G(\mathbf{r}|\mathbf{r}')\sigma(\mathbf{r}')ds' = \varphi(r) \qquad (2)$$

$\sigma(\mathbf{r}')$ is the unknown charge distribution over a conducting surface, or polarisation charge on a dielectric surface. $G(\mathbf{r}|\mathbf{r}')$ is known as a Green's function. It describes the contribution of a charge at $\mathbf{r}'$ to the voltage at $\mathbf{r}$. By summing all the contributing effects, due to all the charges, the total potential is obtained.

The surface charge distribution is conveniently solved by using the Boundary Element Method (BEM) [4,5]. The elements are needed to be only over the surfaces, the far-field conditions being automatically handled by the Green's function.

Once these parasitic values are known, the transmission line systems may be developed. An accepted mathematical approach is through the solution of an eigenvalue problem [6]. This approach yields modes with differing velocities and voltage patterns distributed over the tracks.

For example, if two tracks are placed on a dielectric slab over a ground plane we have two modes: an odd and an even mode. The odd mode has a voltage distribution proportional to 1V and –1V and the even mode voltage distribution is proportional to 1V and 1V. Imagine the electric flux lines streaming from the positively to the negatively charged track and it becomes clear that much of the energy is distributed throughout the air and consequently, the velocity of propagation of this mode will approach that of the signal velocity in free space. On the other hand, the even mode (defined by a voltage distribution proportional to 1V and 1V) will experience electric flux mainly streaming down from the tracks to the ground plane. Clearly, most of the energy is thus located within the dielectric and so this mode will propagate with a velocity approaching that of an electromagnetic signal within the dielectric, i.e. reduced by a factor $1/\sqrt{\varepsilon_r}$ where ε_r is the relative permittivity or dielectric constant. If a cluster of eight wires (a bus, for instance) are in proximity, then there will be eight modes of propagation, each with its own propagation constant.

The PCB has to be modelled as a network of such multiconductor, coupled transmission-line systems and at each junction between such subsystems, a scattering matrix is required to guarantee continuity of currents and voltages. It is important that, before making an acquisition decision, the SI/EMC engineer should ensure that the tools being considered satisfy these and other algorithmic subtleties in order to guarantee robust and accurate algorithms.

The Boundary Element Method

Whatever methodology is used, it is important that it be embedded within the software so that engineers can concentrate on their electronics design problems and need not be concerned with the mathematical and algorithmic subtleties. Nowadays, the preferred technology underlying signal integrity (SI) and electromagnetic compatibility (EMC) tools is based upon the integral equation method using Green's functions. Using this method, conductors and dielectric interfaces are divided into boundary elements over which the free and polarization charges and currents are computed. Use of a higher-order boundary element method (BEM) yields great accuracy and reliability. Moreover, additional accuracy results because the method directly calculates these surface charges and currents. Parasitic inductances and capacitances are directly related to these surface charges and currents. Finite difference and finite element methods result in fields in space (with artificial boundaries needed to truncate the regions) and numerical differentiation (with significant error introduced) needed to produce the surface charges. It is these charges and currents that are directly related to the computation of these capacitances and inductances that are used for PCB transmission-line modelling.

Many SI and EMC computer simulation tools are based upon the finite element method (FEM). The FEM solves for voltages and currents in the space surrounding the conductor and dielectric structures and requires a calculation grid to be extended well beyond the structures if reasonable accuracy is to be achieved. In order to yield reasonable analysis times, arbitrary limits must be applied to the extension of the grid into space and this results in significant calculation error when the charges and currents are computed. Other FEM techniques – such as "absorbing boundary conditions" – are used in an attempt to compensate for the selection of what is often considered to be an inappropriate technique for electronics applications. However, the FEM is preferred for high-power equipment applications (such as magnetics analysis for power transformers and rotating machinery) and in conjunction with the BEM for detailed power and ground plane modelling in PCBs..

Some SI tools forsake field analysis altogether and depend entirely on approximate mathematical equations to estimate parasitics. This approach yields very poor accuracy and usually unacceptable results. The boundary element methodologies favoured are generally considered to be the most accurate available. If these methods are applied diligently, wave shapes can be simulated within a few percent of laboratory measurement. Inattention to these mathematical subtleties result tools that could produce errors of over 10%. While these greater errors may have been acceptable when rise and fall times were of the order of 2 ns to 3 ns, they are not viable with today's sub-nanosecond rise times and the resulting gigahertz signal harmonic content.

These methods not only result in excellent accuracy, but also stable matrices and computational efficiency.

The Simulation Technique

PCB layout design files include specification of stackup, track layout details, components etc. The simulation tool needs to be able to read this data in and interpret it. Component part numbers need to be interpreted as electrical models. To this end, Spice and IBIS models are preeminent. IBIS (Input Output Buffer Information Specification) is a method of providing I/O device characteristics through

V-I data without disclosing any circuit or process information. It is used as a behavioural modelling specification suitable for transmission-line simulation of digital systems and is applicable to most digital components.

After reading in the PCB design data, using an appropriate layout interface, the following steps are performed automatically:

- The time-domain currents are simulated for all (or, if requested, a subset) of the nets.
- A Fast Fourier Transform (FFT) is performed to provide the harmonic content of the time-domain waveshapes.
- The nets are numerically broken down into elemental antenna segments taking into account location and direction of the segments.
- Emissions from pins and vias as well as from the transmission line nets ought to be accounted for. This means that the simulator ought to show emissions even when the PCB is clad in copper sheets, i.e. stripline.
- Using the Law of Biot-Savart, the values of H_x, H_y and H_z are computed by integration over all current elements at any arbitrary height (say 5 mm) above the board.
- The software should then map out the highly-radiating "hot" areas at each frequency.
- It should then highlight the nets that are the principal contributors to establishment of the hot areas. In this way it would point out the wires that have to be dealt with.
- Finally, the simulator should allow the user to perform a variety of termination what-if scenarios to determine the best course of action.

Electromagnetic Emissions

Now we need to deal with signal integrity issues to solve the problem. You cannot solve EMC problems without dealing with signal integrity. Therefore, the simulator should be able to deal with both SI and EMC.

There are three principal signal-related causes of emissions:

1. pulse-repetition frequency, i.e. the clock frequency;
2. signal edge rate; and
3. signal ringing due to mismatch.

A net that encircles a region (i.e. one that is "loopy") will cause more trouble than one that is straight even over a considerable distance.

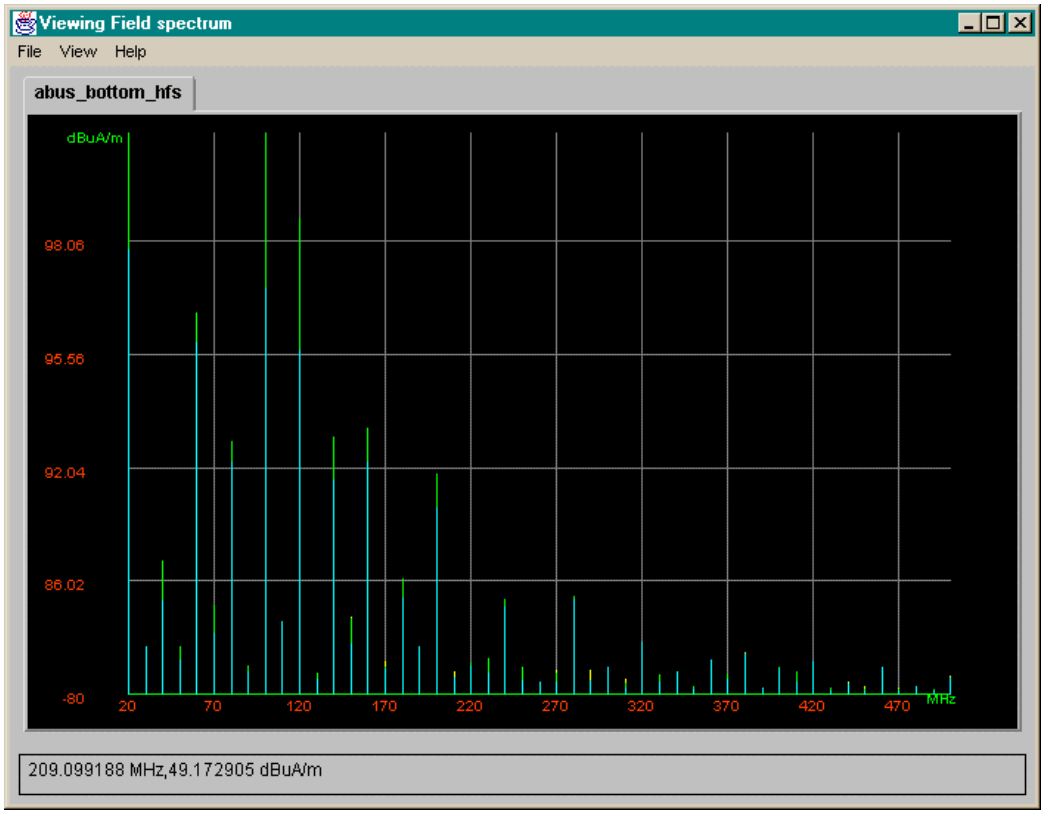


Fig. 1 Maximum magnetic field (H_x, H_y and H_z) spectrum, at a height of 5 mm. 20 MHz clock.

Emission problems will be indicated by high spectral values that can be observed in Figure 1. For example:

- If the clock period is 50 ns (i.e. 50 ns/cycle), the fundamental harmonic is 20 MHz. High clock rates cause dominant spectral values at corresponding frequencies. If the signal is symmetrical in time, the odd harmonics will occur, e.g. 20 MHz, 60 MHz, 100 MHz etc. The 40 MHz, 80 MHz … harmonics will be nonexistent or (in practice) much smaller. The magnitude of these harmonics depends upon the rate of switching charge transferred (i.e. the edge rate) and therefore the magnitude depends upon the technology employed. Edge rate is largely technology dependent.
- If a voltage signal edge rate (i.e. the signal rise or fall time) is 2.5 ns, expect capacitive charging (i.e. unidirectional current transfer) to last for this duration. This corresponds to one-half cycle of the current waveform. Therefore, for the full 5 ns cycle, an associated fundamental current harmonic is expected at 200 MHz. Currents cause emissions and so expect significant emissions at that frequency. Reducing the slope of the leading edge will reduce the rate of charge transfer (i.e. current strength) and resulting emissions.
- Ringing, due to termination mismatch, is identified by signals superimposed upon the voltage waveform. The period of oscillation depends upon the pin-to-pin length from driver to terminations and the velocity of propagation of the signal. (Signal integrity simulation provides this information.) We like to see serious ringing die down (due to attenuation over several multiple pin-to-pin traverses of the signal) during the time of the rising-edge. Therefore, a slow edge will keep the signal peak from being deformed (i.e. overshoot and undershoot violations – false triggering!) by excessive ringing.

High-Emission Regions

Figure 2 shows the highly radiating regions on a printed circuit board. The two most significant nets, that are the cause of the problem, are highlighted. Note that the maximum magnetic field they produce is 97.17 dBuA/m. (If logarithmic units are not wanted, the results can be presented in units of A/m.)

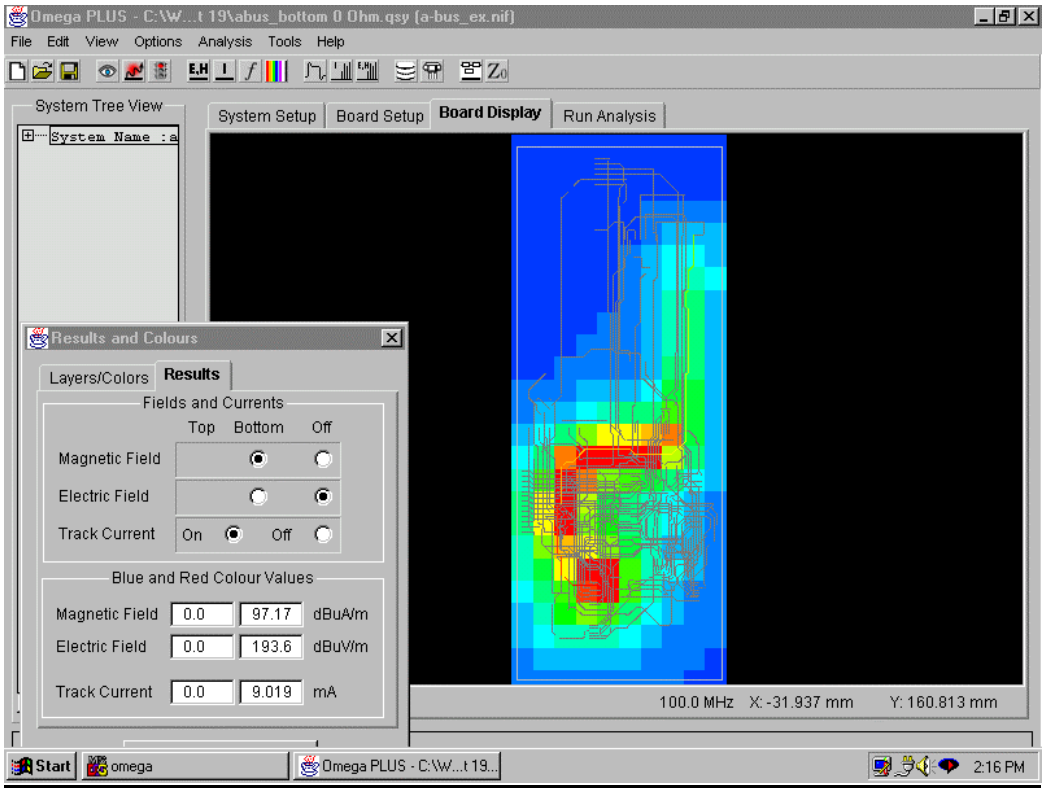


Figure 2. PCB magnetic field mapping and highlighted principal nets that are the cause of most emissions.

Figures 3 and 4 show the voltage and current waveforms, of the most significant (orange) net, at all connected pins. The steep rising edge is due to the semiconductor technology edge rate plus ringing due to reflections from the net terminations. You can see the bump on the rising edge where the effect of ringing kicks in and the signal overshoot is obvious.

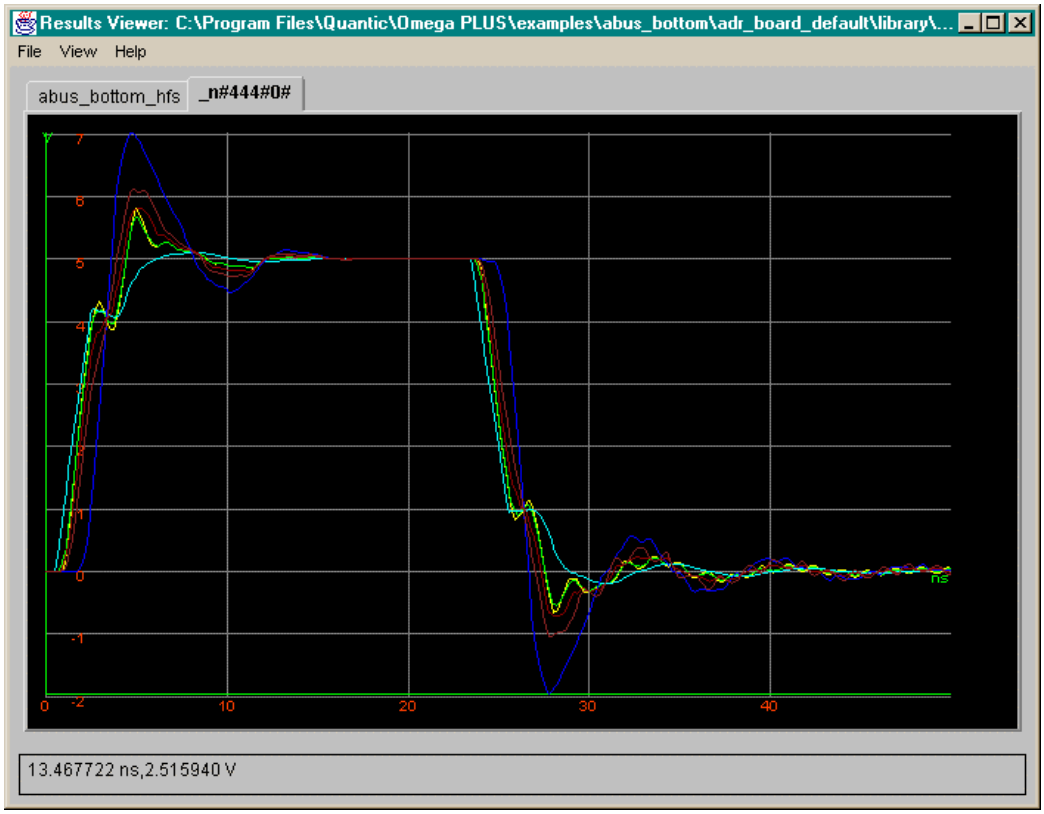


Figure 3. Voltage waveshapes at all pins on the dominant net.

The effective voltage edge rate is seen to be approximately 5 ns. Correspondingly, the current cycle time, at the leading edge – and it looks almost like a sine wave – is 10 ns. These observations correspond to emissions at 100 MHz.

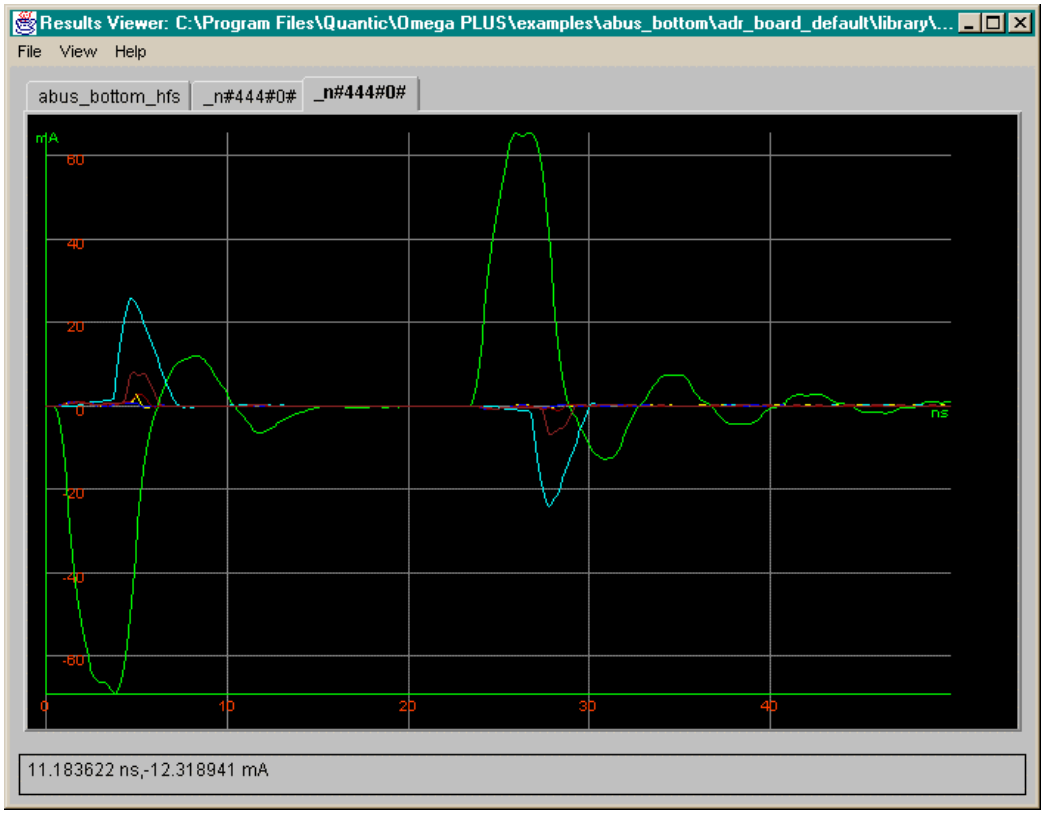


Figure 4. Current waveshapes within all tracks along the dominant net.

The emissions spectrum chart (Figure 1) shows a peak emission at that same frequency of 100 MHz!!!

We therefore conclude that this emission is due to the rapid edge rate (due to the combination of the semiconductor technology and the transmission-line ringing) and not due to the pulse repetition frequency.

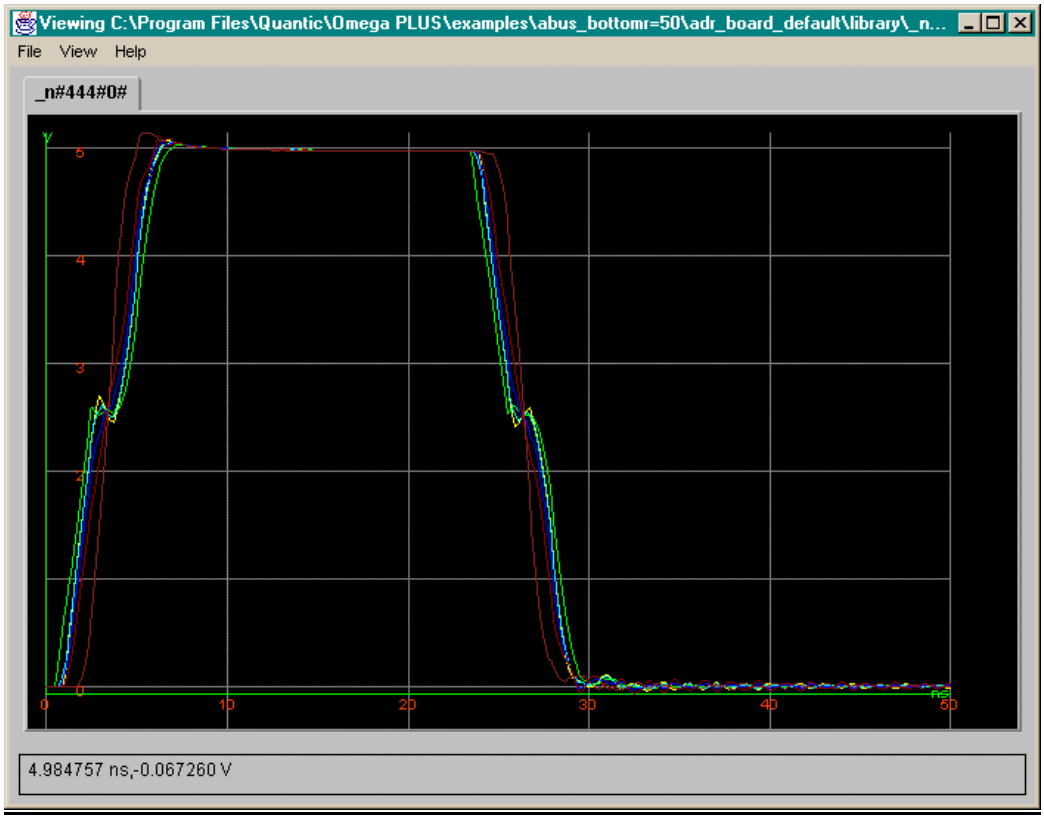
Brain Surgery

Adding ferrites, absorbing materials and sealing enclosures tightly is a ham-fisted approach to solving EMC problems. These techniques are akin to dipping the PCB into a bath of molten solder to certainly contain emissions!!

The elegant solution is to rectify the problem at the source. (See also Archambeault [7].] Go to the identified perpetrator of the emissions and correct the problem there. This is more like brain surgery using intra-operative technology.

We have now identified the problem net. And we know that the root cause of the emissions is due to steep pulse edges. Whereas ringing can be rectified by adding a matching resistor to terminations, modifying the edge rate can be accomplished by a series resistor at the driver pin. In a practical way, this can be viewed as a means of increasing the equivalent driver RC time constant – thus slowing

down the edge rate. In fact, the driver resistor can also reduce ringing by absorbing most of the reflected signal upon its return from the termination. Figure 5 shows the effects of adding resistors to the driver and termination pins. It is apparent, by comparison of Figures 3 and the left-hand graphic of Figure 5, that the edge rates have been reduced significantly.



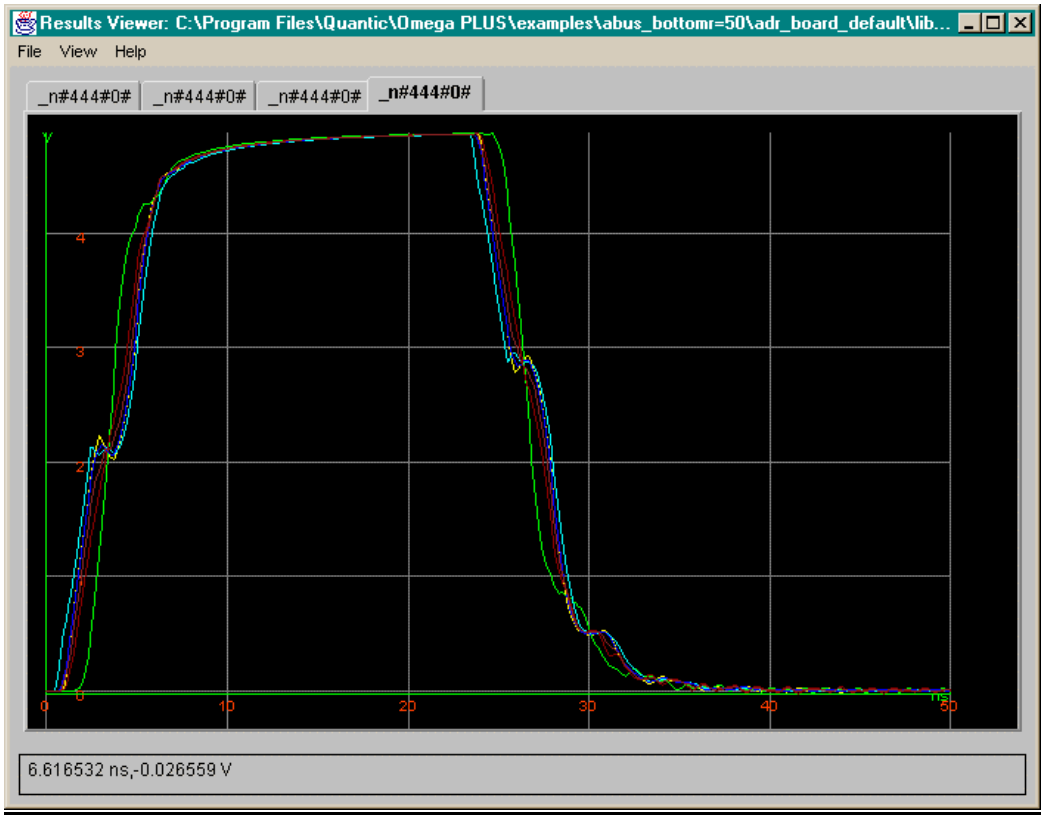


Figure 5. 50 Ohm resistor added in series with the driver pin (top) and a 75 Ohm resistor added in parallel with the receiver pin (bottom).

In the top figure, a 75 Ohm resistor was inserted in parallel with the most-distant receiver. The edge-rate is hardly affected, in comparison with Figure 3, and some ringing is still evident. The first peak occurs at the same time as the bump seen in the left-hand figure. Both of these events are clearly due to ringing. If necessary, this could be rectified by inserting matching resistors at the other terminations on the net. Or the 75 Ohm resistor could be replaced with one of another value.

It is a simple matter to do these emission-reduction what-if scenarios with a terminations editing facility in the simulator. In Figure 6, one simply selects the net in question and then its driver pin. For example, in the top graphic of Figure 5, 50 Ohms was inserted in series with the driver. The bump on the rising edge is still evident due to the reflected signal.

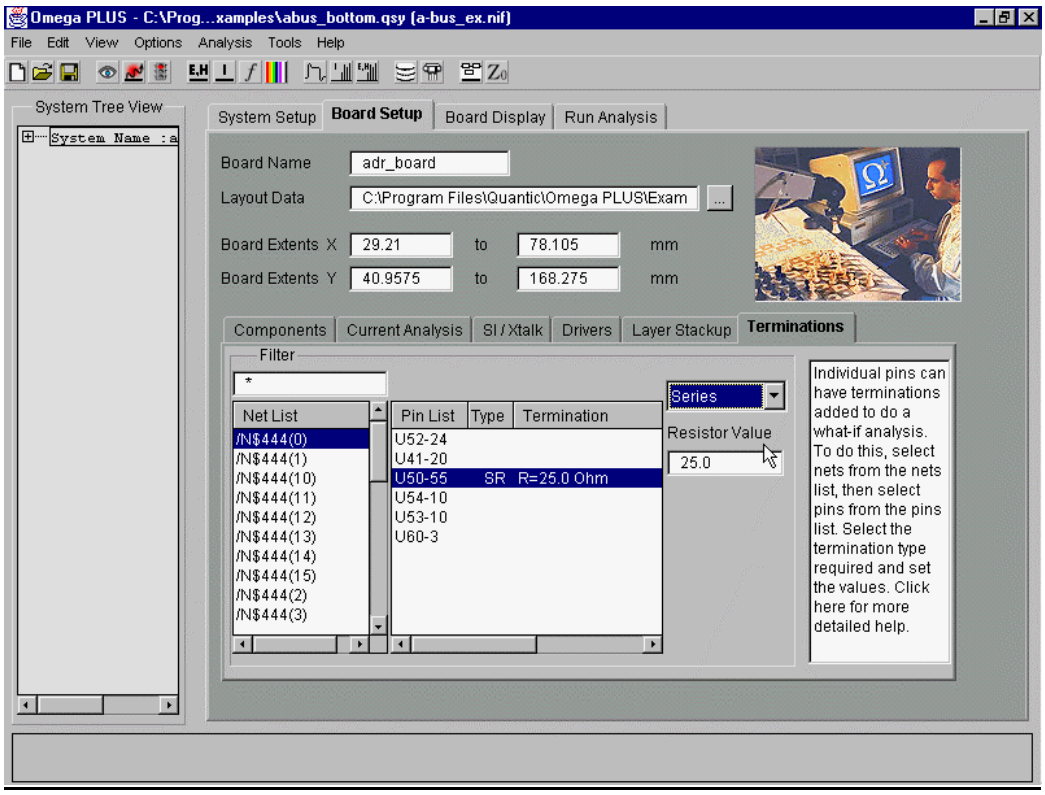


Figure 6. Editing a termination resistor value to suppress emissions.

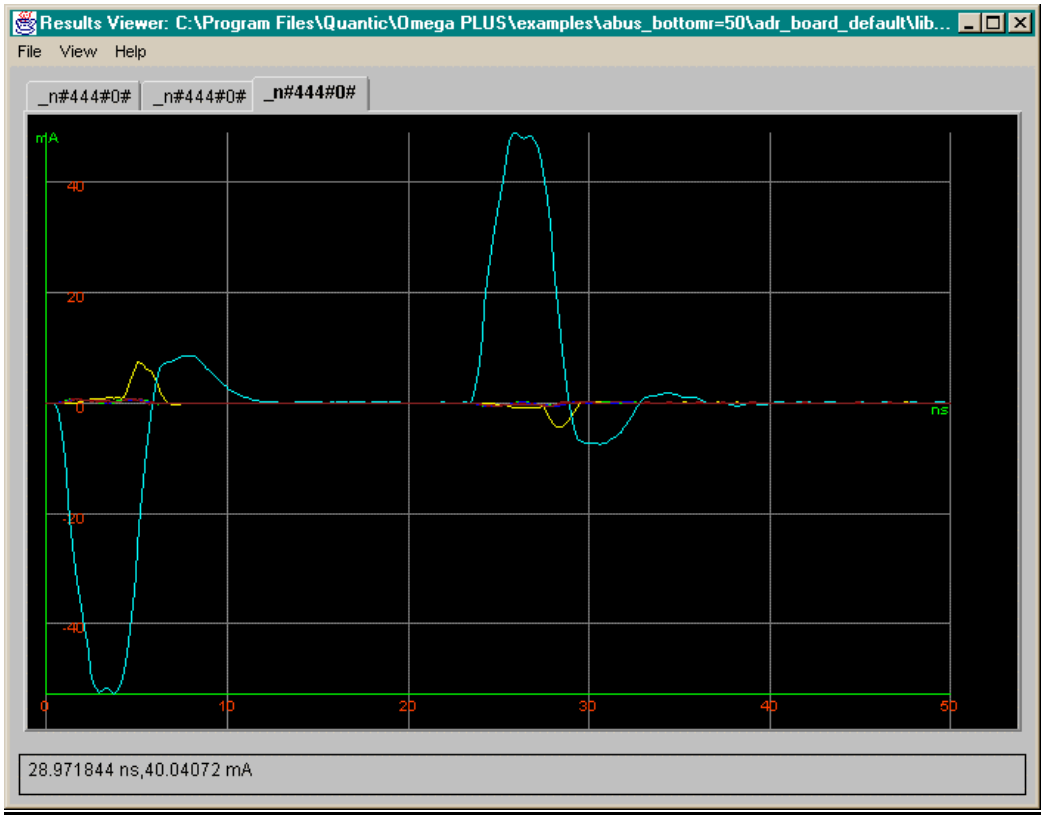


Figure 7. Current waveforms reduced. 25 Ohm resistor in series with the driver pin. Compare with Figure 4.

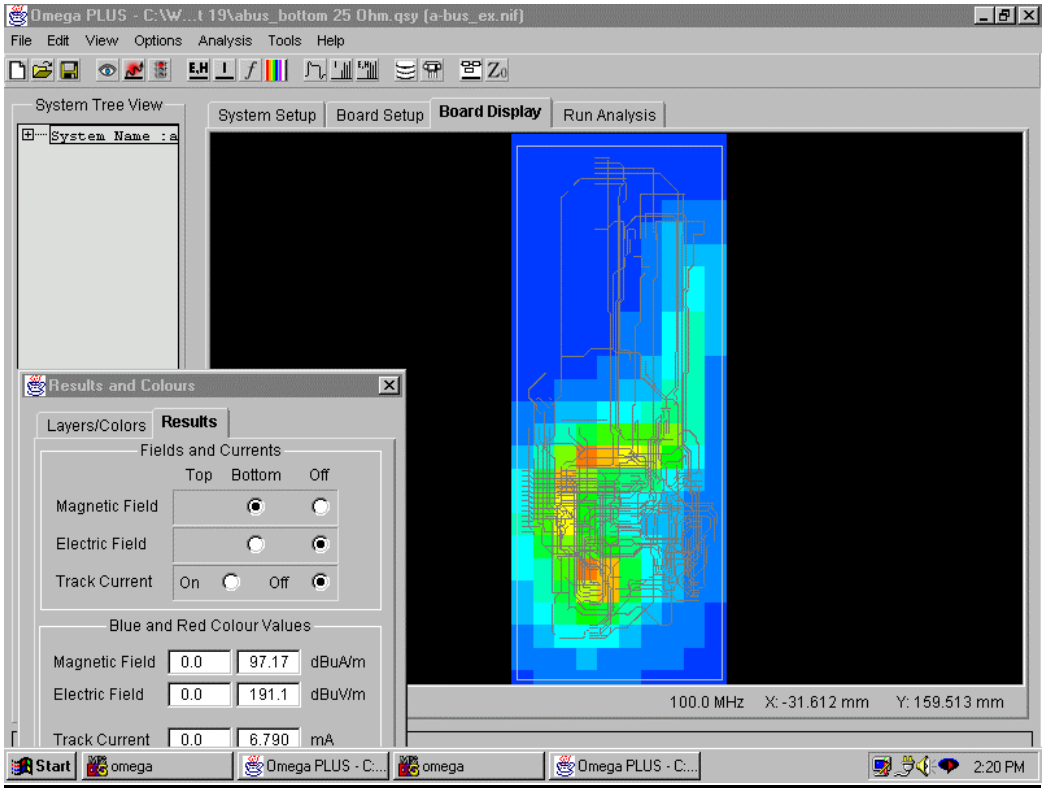


Figure 8. Reduced emissions with 25 Ohm resistor placed in series with the driver pin. Compare with Figure 2.

Comparison of Figures 4 and 7 indicates a significant reduction in the line currents experienced at the pulse edges.

Comparison of Figures 2 and 8 shows a reduction of emissions due to the inclusion of the 25 Ohm resistor. Other Omega PLUS output data indicates a reduction of over 2 dBuA/m. Increasing the resistor to 50 Ohms causes an additional 3 dBuA/m reduction.

Although there is no direct and simple relationship between near-field and far-field values, in a given design environment, experience will dictate what field strengths are acceptable in practice.

What Else to Consider

More sophisticated techniques to consider involve grading of track dimensions, spreading of dominant emissions frequencies so that clock, edge and ringing emissions do not accumulate and other techniques, rerouting and other design alterations. Adequate SI and EMC simulation tools allow designers and engineers to prevent problems at the design stage, to identify problem nets as a result of laboratory testing, to develop physical intuition, and to try corrective scenarios. The goal is to avoid problems and to meet product deadlines.

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