 By Julian Hayes, Wolfson Microelectronics

TOP-RATE PERFORMANCE MEANS UNDERSTANDING CLOCKING, POWER SUPPLIES, AND TRANSISTOR-SWITCHING CHARACTERISTICS.

Getting the most from Class D multichannel audio amplifiers

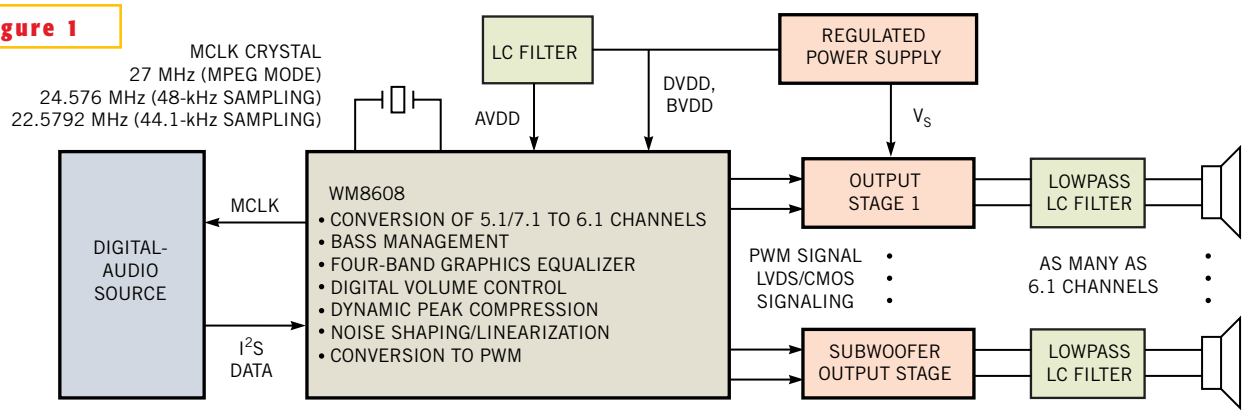
Class D amplifiers have evolved to the point at which they are a viable alternative in most audio applications. However, because their principles of operation differ from those for linear amplifiers, it's worth examining a new set of factors to get the best possible performance from this amplifier class. Clocking, power supplies, and the switching characteristics of the output transistor are areas of concern as problems and potential solutions in Class D performance optimization.

All Class D amplifiers use a square waveform, usually a PWM (pulse-width modulated) signal, to drive the output stage. Passive LC filtering then converts this signal into an analog waveform suitable for a loudspeaker. However, there are different ways to produce the PWM signal in the first place. Some Class D amplifiers compare an analog input signal against a high-frequency sawtooth waveform; others transform digital audio data to PWM in the digital domain. With native digital audio sources, such as DVDs, CDs, and digital broadcasting, the second, all-digital architecture has the advantage of eliminating from the signal path two potential sources of noise: a DAC and an analog comparator (**Figure 1**).

However, digital PWM modulators present their own design challenges. They derive their output signals from a high-frequency internal clock running at a multiple of the master clock rate. Depending on the digital input, the PWM outputs are periodically held high for fewer or more clock cycles before returning to their low state. It's crucial to keep the internal clock clean, because any jitter would cause random variations in the timing of the PWM signal edges, which appear as noise in the analog output. It is therefore preferable to generate it from the system master clock using an on-chip, low-jitter PLL (phase-locked loop).

This method filters out most jitter, as long as the

Figure 1



NOTES:
AVDD: ANALOG SUPPLY—FEEDS ANALOG SUBCIRCUITS OF THE MODULATOR IC.
DVDD: DIGITAL SUPPLY—FEEDS DIGITAL CORE OF THE MODULATOR IC.
BVDD: BUFFER SUPPLY—FEEDS OUTPUT BUFFERS OF THE MODULATOR IC.

The Class D amplifier architecture for native digital inputs can have a different architecture from the older design for analog inputs.

master clock is reasonably clean. Ideally, the master clock should itself be produced on-chip to prevent interference from the switching output stages or to prevent other sources from corrupting it, because the connection between oscillator and PLL remains on-chip. It also eliminates external PLL-filter components, reducing sensitivity to the pc-board layout. Finally, inserting a decoupling filter close to the supply pin that is powering the PLL helps prevent supply noise from affecting it.

OUTPUT-STAGE DESIGN HAS ITS TWISTS

Much like analog amplifiers, Class D output stages can be single-ended with two transistors per channel (half bridge) or of the four-transistor type BTL (bridge-tied load). Designers usually prefer the BTL configuration, because it offers single-supply operation without a dc blocking capacitor (**Figure 2**).

Single-ended output stages require either a large capacitor to remove dc bias from the output or more expensive split supplies. Another advantage of the BTL configuration is that it doubles the output swing (V_{PP}) from V_S (the supply voltage) to $2V_S$, quadrupling the theoretical maximum power P_{MAX}, that can be delivered for a given supply voltage:

$$P_{BTL} = V_L^2/R_L = (2V_S)^2/R_L = 4V_L^2/R_L = 4P_{HALF\ BRIDGE}.$$

In practice, the PWM controller's duty cycle, δ, usually spans about 5 to 95%, constraining the output swing from $2V_S$ to around $1.8V_S$, and resistive losses further reduce power output. You can calculate these values as:

$$P_{BTL} = V_L^2\delta^2/R_L = 4(V_S - 2R_{PARASITIC}I_L)^2\delta^2/R_L.$$

where $R_{PARASITIC}$ includes the on-resistance of one NMOS and one PMOS device as well as the supply's internal resistance, the series resistance of the filter inductors, and pc-board track resistances.

An easy way to maximize output power is to use low-impedance speakers. For example, a 4Ω load can draw twice as much power as an 8Ω speaker for the same supply voltage. However, this method slightly decreases power efficiency, because parasitic resistances become more significant compared with the load itself.

Dynamic peak compression makes audio signals sound louder without resorting to a more powerful output stage. Essentially, it amplifies the signal in the digital domain, dynamically adjusting the gain to prevent clipping. However, rapid gain changes can audibly distort low-frequency signals. Recently introduced PWM modulators are overcoming this issue by making the peak compressor's decay time frequency-dependent. This step allows the gain to change rapidly for high-frequency signals and slows it for the lower part of the audio range.

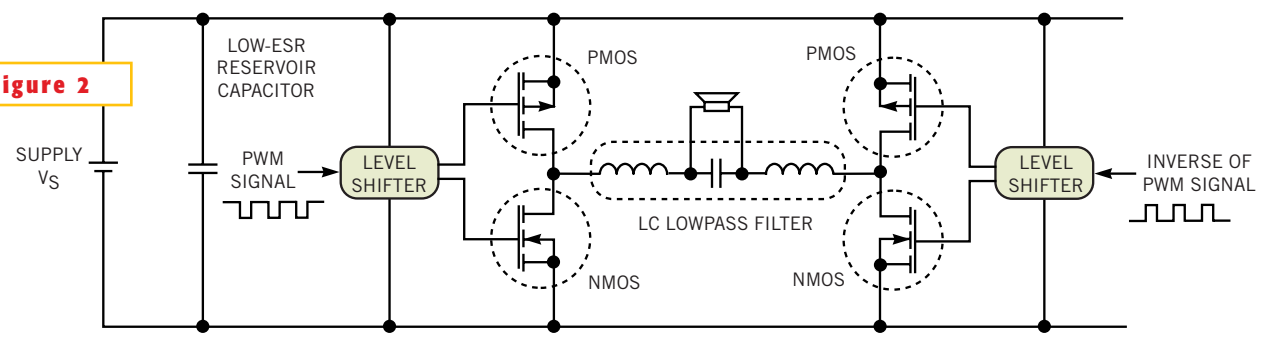
Selecting appropriate components for the output stage is critical, because their characteristics have a strong effect on system performance. First, the power MOSFETs need to withstand the voltage and current they are expected to handle. Because the rapidly switching PWM signal can induce a back-EMF (electromotive force) in the output-filter inductors, the maximum rated drain-source voltage should be at least 25 to 50% higher than the supply voltage. Second, the on-resistance of the power MOSFETs causes heating and lowers power efficiency, so it should be as low as possible. Commonly used speakers with impedances of 4 or 8Ω require on-resistance to be well below 0.2Ω to keep resistive losses reasonably small.

Switching delays are another important parameter for selecting output devices. PWM pulse widths usually range from hundreds of nanoseconds to a few microseconds. To preserve signal integrity, the switching delay of the output stage (power MOSFETs plus level shifters) should be smaller than the minimum PWM pulse width. A less obvious potential issue is the matching of switching characteristics between transistors. If, for example, an NMOS device turns on significantly faster than its PMOS counterpart switches off, the on-times of both devices may overlap for a short time on signal edges. With both devices conducting, the power supply essentially short-circuits, leading to reduced power efficiency, increased heat dissipation, and a possible supply-voltage dip, which would distort the audio signal.

Finally, designers should pay attention to the MOSFET gate capacitance. A large capacitance causes RC delays that slow the switching of the transistors. Moreover, it also increases power dissipation and heating in the level shifter driving the MOSFET. For the same reasons, the level shifter's input capacitance should also be small.

Several manufacturers offer integrated output stages that you can connect directly to a PWM modulator. These ICs,

Figure 2



The H-bridge output has the virtue of single-supply operation without a dc blocking capacitor.

which generally include four matched-power MOSFETs, also manage the level shifting of the PWM signal from the modulator output levels to higher voltages that can correctly switch the power devices. In addition, they usually provide built-in short-circuit and overload protection.

PROVIDING POWER IS ALSO CRITICAL

In many ways, the increasing use of switching power supplies over traditional linear supplies mirrors the rise of Class D in amplifiers. Both owe their growing popularity to their high power efficiency, compactness, and reduced cooling requirements. Using a switching supply, therefore, helps designers reap the full benefits of Class D technology. Nevertheless, when cost is the overriding consideration, regulated linear supplies can power Class D amplifiers.

One potential concern with switched supplies is EMI (electromagnetic interference) due to the rapid switching of large currents. This problem is exacerbated when switching frequencies in the supply and the amplifier intermodulate, producing tones that may be audible in the output. Some PWM controllers offer the ability to synchronize an external power supply with the on-chip PWM modulator, eliminating intermodulation. However, most power supplies on the market today do not yet allow for synchronization. Closer cooperation between audio-IC and of power-supply vendors is necessary to bring power-supply synchronization into the mainstream.

No matter what type of supply you use, Class D amplifiers are much more sensitive to the quality of the power supply than their linear counterparts. So, although Class D technology will almost certainly reduce power requirements by 50% or more, the actual design of the supply tends to be rather more intricate. The reason is simple: With nothing but switches (power MOSFETs turned fully on or fully off) between the supply and the output, any mains or audio-band ripple on the supply rails will modulate the output signal. In other words, all-digital Class D amplifiers have a PSRR (power-supply-rejection ratio) of 0 dB; they essentially use the supply as a voltage reference.

Good load regulation—not just at dc, but across the entire audio band—is therefore indispensable; poorly regulated supplies cause harmonic distortion. A number of manufacturers provide floating regulators that you can add to supplies to improve load regulation. Using a separate regulator for each amplifier output can also reduce crosstalk between audio channels.

Another key criterion for the power supply is its ability to handle transients. For the output stage to accurately reproduce the PWM signal, the supply must be able to rapidly increase or decrease its current output and without ringing or a drop in the output voltage. Linear amplifiers are less demanding in this respect, because the bandwidth of the output stage is limited to the audio range. Thus, a supply that performs well in a linear system may be unsuitable for Class D.

Reservoir capacitors are the most critical components determining the supply's transient behavior. First, they need to hold enough charge to prevent a current surge from causing the supply voltage to drop until the regulator kicks in. (A fast regulator helps keep the capacitor reasonably small.) Second, because any parasitic resistance or inductance impedes a rapid delivery of the stored charge, you must use low-ESR (effective-series-resistance) capacitors. But adding a small, low-ESR capacitor in parallel with a larger, conventional electrolytic capacitor is insufficient. Because all the output power is delivered in short bursts, all of the capacitance needs to have low ESR. Parasitic resistances and inductances in pc-board copper tracks are equally detrimental, and you should minimize them by placing the reservoir capacitors as close as possible to the output stage.

Alleviate demands on the transient behavior of the supply by arranging for the MOSFETs in the output stages to switch at different times. To this end, recently introduced PWM controllers feature a PWM phase-shift function that introduces a fixed delay between the PWM

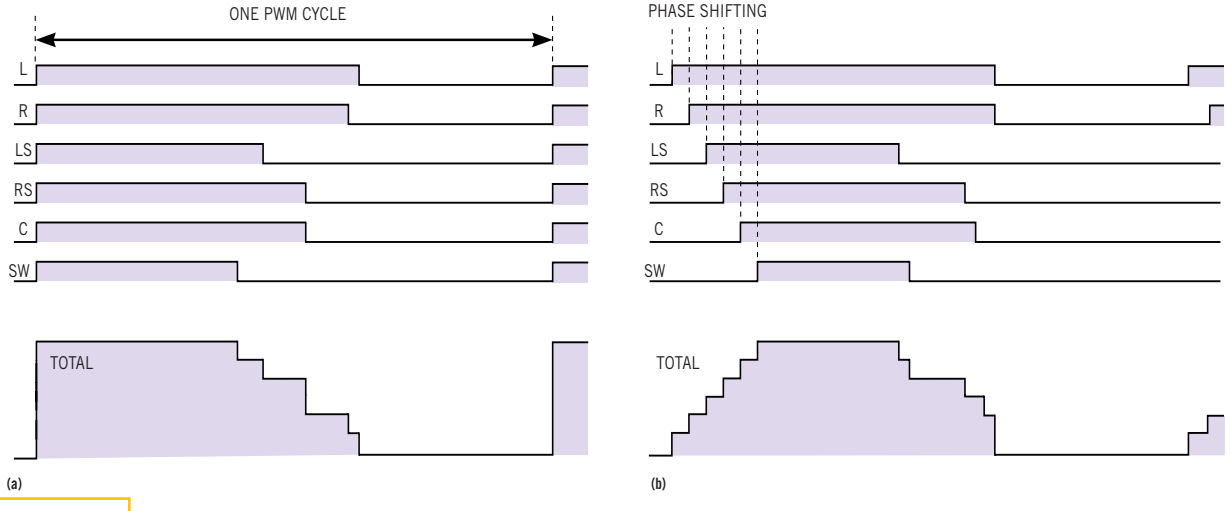


Figure 3

A multichannel Class D amplifier (a) can minimize transient current demand from the power supply if you introduce phase shift in the PWM signal (b).

signals for each output channel (**Figure 3**). At a fraction of a PWM cycle, this delay is far too short to make an audible difference to the output, but it spreads switching transients around the PWM cycle. In a system with six channels, this technique significantly diminishes the maximum instantaneous load current and reduces crosstalk.

THEN THERE'S THE LAYOUT

EMI is invariably a concern in Class D-amplifier design. Wires carrying high-power PWM signals emit electromagnetic radiation at the PWM frequency and its harmonics, well into the radio bands. Long, unshielded speaker cables, in particular, behave essentially like antennas. The reconstruction filters therefore play an important role in achieving compliance with relevant regulations. Designers often face a trade-off whereby a filter with a low cutoff frequency both suppresses EMI and attenuates the high end of the audio spectrum, but a high cutoff preserves a flat frequency response at the cost of increased EMI. High-order filters can do both but are more expensive and reduce power efficiency. Digital-speaker equalizers offer a way out. When programmed as a treble boost, they make it possible to use low-order reconstruction filters with a low cutoff and still keep the frequency response flat across the audio range. You can also use different equalizer settings to match the system to speakers with different impedances.

SHORT, WIDE COPPER TRACKS MAKE THE AMPLIFIER MORE EFFICIENT BY CUTTING RESISTIVE LOSSES.

Inside the amplifier, reduce EMI by keeping the supply rails and the connections between output stages and filters as short as practicable. If possible, these components should be on the same pc board as the power supply. Short, wide copper tracks also make the amplifier more efficient by cutting resistive losses. In multichannel systems in which the power MOSFETs make it difficult to place them all close to the supply, a star connection with a low-ESR reservoir capacitor at each end is ideal for preventing crosstalk.

The only part of the system that you can place at some distance from the other circuitry is the PWM controller. To prevent interference from other system components from inducing jitter in the PWM signals, some PWM controllers offer LVDS (low-voltage differential signaling), in which each line terminates with a 100Ω load. LVDS also reduces electromagnetic emissions and RC delays due to the long signal runs.

Three key metrics for consumer-audio amplifiers are THD (total harmonic distortion), SNR (signal-to-noise ratio), and power efficiency, in which Class D technology indisputably has the edge over analog. Regarding noise, Class D today is on a par with most analog amplifiers in the consumer market. Moreover, the SNR bottleneck is often not the amplifier but the encoding of the source data. For example, for traditional CDs with 16-bit data words, quantization noise limits its SNR to a theoretical maximum of 96 dB. With faster PWM switching, the SNR of Class D amplifiers may improve further in future. The key issue is whether the power supply and switching transistors can keep up with the switching speed. THD remains the most critical metric, although manufacturers have made much progress in this area. With the latest generation of PWM controllers and stable, well-regulated supplies, mass-market devices at low output powers have demonstrated THD levels to as low as −80 dB (0.1%). Most likely, future improvements will hinge on power supplies and output stages. These two components together dominate THD and should ideally be co-designed as one unit.□

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